IT700 MAIN FEATURES

- Low-cost powerline communication (PLC) modem and application solution in a single chip
- Incorporates Yitran's high performance Data Link Layer (DLL), Network Protocol (Y-Net) and extremely robust Physical Layer (PHY)
- Extended 8051 microcontroller with 256KB Flash for protocol stack and application
- **Protocol Controller Architecture** version: pre-programmed with communication stack
- **Open Solution Architecture** version: allows user to program application code together with the communication stack.
- Full home coverage even under adverse line conditions
- HomePlug® Command and Control ready
- Fully backward compatible with IT800 Series

APPLICATIONS

- Smart Grid Applications:
  - Automated Meter Reading (AMR)
  - Advanced Meter Management (AMM)
- Energy Management:
  - Smart Home & Building Automation
  - Home Appliance Control & Diagnostics
  - Security and Access Control
  - Environmental Control
- Commercial Applications:
  - Street Light Control
  - Vending Machine Control
  - Signage Control

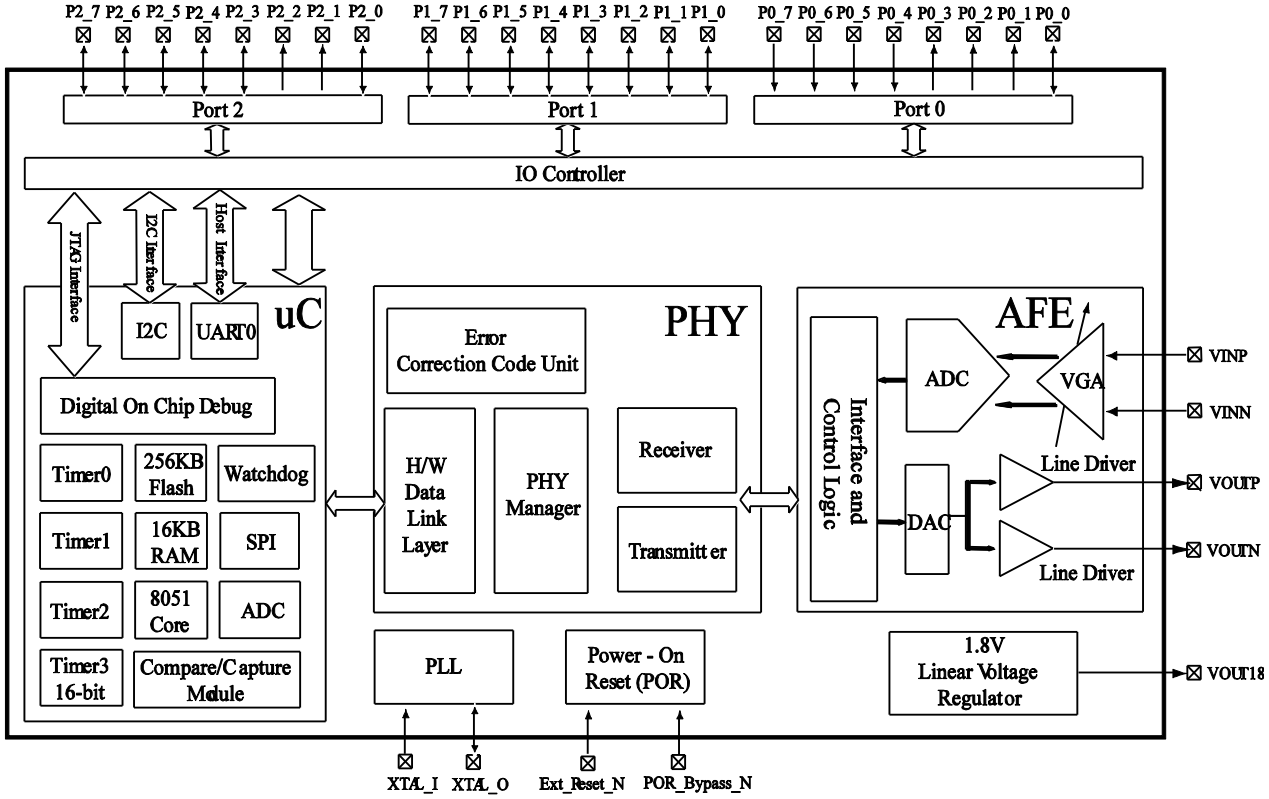

Figure 1: IT700 Block Diagram

1. Communication Layer Features

LAYER 1 (PHY)

- Patented DCSK modulation
- High immunity to signal fading, noise, impedance modulation and phase/ frequency distortions
- High in-phase and cross-phase reliability
- Forward short-block soft decoding error correction mechanism and CRC-16
- Complies with FCC, ARIB and EN50065-1-CENELEC regulations
- FCC and ARIB bands bit rate:
  - 7.5Kbps Standard Mode (SM)
  - 5.0Kbps Robust Mode (RM)
  - 1.25Kbps Extremely Robust Mode (ERM)
- CENELEC band bit rate:
  - 2.5Kbps Robust Mode (RM)
  - 0.625Kbps Extremely Robust Mode (ERM)

LAYER 2 (DLL)

- Up to 1023 logical networks and 2047 nodes per network
- Acknowledged and Unacknowledged data transmission services
- Re-transmission mechanism
- Automatic rate control
- Adaptive Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) channel access
- Fragmentation and re-assembly to support full Ethernet packet transmission

LAYER 3 (NETWORK)

- Supports 1000 different, overlapping networks
- Supports 2000 nodes in each network
- Master-Slave and Peer-to-Peer Network Configurations
- Plug & Play Network Setup
- Automatic logical network creation
- Automatic node address allocation
- Automatic and adaptive Routing Service (Tree topology)
- Network Parameter Recovery
- Failure Detection
- Full security Suite including AES 128-bit encryption with 32 bit authentication

2. IT700 General Description

The IT700 is a highly integrated System-on-a-Chip (SoC) powerline communication (PLC) modem. It incorporates Yitran's extremely reliable Physical Layer (PHY), high performance Data Link Layer (DLL) and Yitran Network Layer (Y-Net) protocol.

An integrated microcontroller with extended 8051 core, 256KB Flash memory, 16KB RAM and 24 general purpose I/Os implements the protocol stack and offers the required flexibility to implement various protocols and applications. The microcontroller's UART interface provides the connection to an external Host and application controller. The I^2C interface connects an optional external EEPROM for configuration parameter storage.

The IT700 modem core uses Yitran's patented Differential Code Shift Keying (DCSK) advanced spread spectrum modulation technique. DCSK enables extremely robust communication over existing electrical wiring with data rates up to 7.5Kbps. In addition to the inherent interference immunity provided by DCSK modulation, the device utilizes several mechanisms for enhanced communication robustness, such as a patented forward short-block soft-decoding error-correction algorithm and special synchronization algorithms.

The integrated Analog Frontend provides differential inputs and line driver outputs to connect via an external line filter and coupler to the power transmission lines. An integrated Phase Locked Loop Circuit allows the operation of the IT700 with a choice of different crystal oscillators. An integrated Power On Reset (POR) circuitry eliminates the need for any external reset components and provides an autonomous, safe power-up and power-down reset to the chip. The integrated 1.8V voltage regulator allows the IT700 to operate from a single 3.3V supply voltage.

The IT700 complies with worldwide regulations (FCC part 15, ARIB and CENELEC bands) and is an ideal solution for a variety of "No New Wires" narrowband PLC applications.

The IT700 will be available in two versions:

The **Protocol Controller Architecture** version has Yitran's Y-Net network layer protocol (layer 3) pre-programmed into the 8051 microcontroller's Flash memory. A UART interface and simple command language provide seamless connection to an external Host controller and simplify application development. In this version you have no access to the microcontroller's unused memory space, peripheral functions and general purpose I/Os.

The **Open Solution Architecture** version allows you to utilize the IT700 microcontroller's peripheral functions, such as timers, interrupts, communication interfaces, A/D, spare memory resources and general-purpose I/Os to implement your own application code, thereby eliminating the requirement for an external host controller. An Application Programming Interface (API) enables the easy integration of your application code with Yitran's Network Layer code.

This advanced information document covers the Protocol Controller Architecture version only; release of the Open Solution Architecture version is scheduled for a future date.

3. Pinout and Pin Description

3.1 Pinout

The following figure shows the IT700 QFN56 lead-free package pinout:

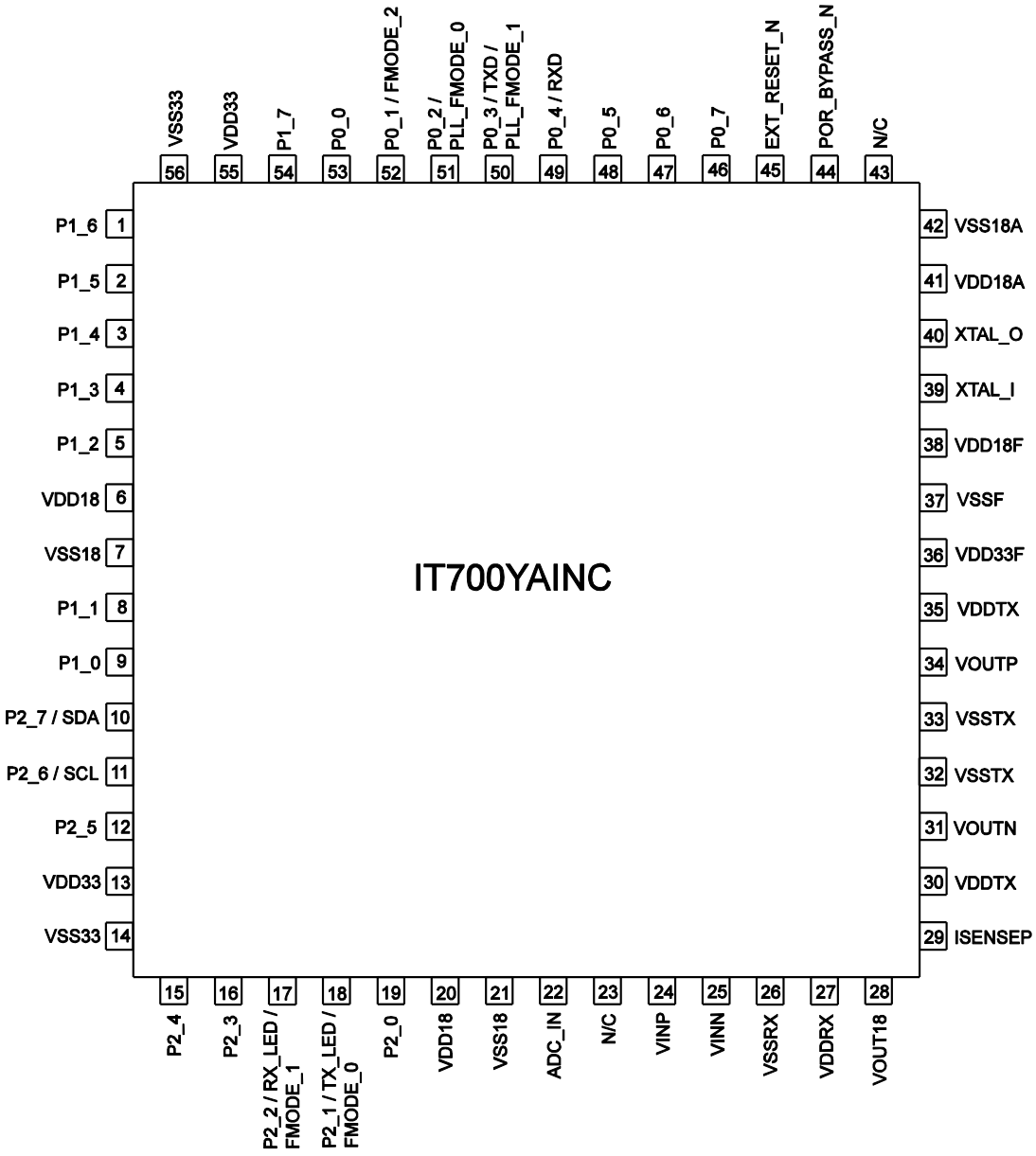

Figure 2: IT700 QFN56 Package Pinout

3.2 Pin Description

The functionality of the IT700 pins is described in Table 2. The pin type format used is xx/yy and the options for the xx and yy fields are shown in the following table:

Table 1: Pin Type Syntax

xx	Description
I	Input
O	Output
IO	Input or Output

yy	Description
PD	Internal Pull-Down
PU	Internal Pull-UP
A	Analog

Table 2: IT700 Pin Description

Pin #	Pin Name Alternate Functions	Type	Description
1	**P1_6** INT1	IO/PU	General-purpose input/output External Interrupt input
2	**P1_5** INT0	IO/PU	General-purpose input/output External Interrupt input
3	**P1_4** CAPTURE0 INT3	IO/PU	General-purpose input/output Timer T2 Capture/Compare input 0 External Interrupt input
4	**P1_3** INT2	IO/PU	General-purpose input/output External Interrupt input
5	**P1_2** T2EX INT6	IO/PU	General-purpose input/output Timer T2 External event reload input External Interrupt input
6	**VDD18**	Power	+1.8V supply voltage: must be connected to VOUT18 (pin 28)
7	**VSS18**	Power	Digital Ground
8	**P1_1** T2 INT5	IO/PU	General-purpose input/output Timer T2 external clock or gated clock input External Interrupt input
9	**P1_0** T3EX	IO/PU	General-purpose input/output Timer T3 External event reload input
10	**P2_7** SDA	IO/PU	General-purpose input/output I^2C Serial Data (SDA)
11	**P2_6** SCL	IO/PU	General-purpose input/output I^2C Serial Clock Line (SCL)
12	**P2_5** SCK	IO/PU	General-purpose input/output SPI Master Clock Output (SCK)
13	**VDD33**	Power	+3.3V supply voltage
14	**VSS33**	Power	Digital Ground

Pin #	Pin Name Alternate Functions	Type	Description
15	**P2_4** MOSI	IO/PU	General-purpose input/output SPI Master Data Output (MOSI)
16	**P2_3** MISO	IO/PU	General-purpose input/output SPI Master Data Input (MISO)
17	**P2_2** RX_LED FMODE_1	O/PU	General-purpose output Receive LED Functional Mode select, Bit 1 (sampled during Reset)
18	**P2_1** TX_LED FMODE_0	O/PU	General-purpose output Transmit LED Functional Mode select, Bit 0 (sampled during Reset)
19	**P2_0** CAPTURE1	IO/PU	General-purpose input/output Timer T2 Capture/Compare input 1
20	**VDD18**	Power	+1.8V supply voltage, must be connected to VOUT18 (pin 28)
21	**VSS18**	Power	Digital Ground
22	**ADC_IN**	I/A	Analog to Digital Converter Input
23	**N/C**	I	Not Connected
24	**VINP**	I/A	Positive Differential Input from powerline coupler/filter
25	**VINN**	I/A	Negative Differential Input from powerline coupler/filter
26	**VSSRX**	Power	Analog Ground
27	**VDDRX**	Power	+3.3V Analog Power Supply
28	**VOUT18**	Power	+1.8V Voltage Regulator Output
29	**ISENSEP**	I/A	Current Sense Input
30	**VDDTX**	Power	+3.3V Analog Power Supply
31	**VOUTN**	O/A	Negative Differential Line Driver Output to powerline coupler
32	**VSSTX**	Power	Analog Ground
33	**VSSTX**	Power	Analog Ground
34	**VOUTP**	O/A	Positive Differential Line Driver Output to powerline coupler
35	**VDDTX**	Power	+3.3V Analog Power Supply
36	**VDD33F**	Power	+3.3V Digital Power Supply
37	**VSSF**	Power	Digital Ground
38	**VDD18F**	Power	+1.8V supply voltage: must be connected to VOUT18 (pin 28)
39	**XTAL_I**	I	External Oscillator Input
40	**XTAL_O**	IO	External Oscillator Output
41	**VDD18A**	Power	+1.8V analog supply voltage: must be connected to VOUT18 (pin 28)
42	**VSS18A**	Power	Analog Ground
43	**N/C**	I/PU	Not Connected
44	**POR_BYPASS_N**	I/PU	Power On Reset (POR) Bypass, active low
45	**EXT_RESET_N**	I/PU	External reset, active low. Only required if POR is disabled
46	**P0_7** TMS TMS_FLASH	I/PU	General-purpose input Microcontroller JTAG Debug interface TMS signal Flash JTAG programming interface TMS signal

Pin #	Pin Name Alternate Functions	Type	Description
47	**P0_6** TDI TDI_FLASH	I/PU	General-purpose input Microcontroller JTAG Debug interface TDI signal Flash JTAG programming interface TDI signal
48	**P0_5** TCK TCK_FLASH	I/PU	General-purpose input Microcontroller JTAG Debug interface TCK signal Flash JTAG programming interface TCK signal
49	**P0_4** RXD	I/PU	General-purpose input UART Receive Data In (RXD)
50	**P0_3** TXD PLL_FMODE_1	O/PU	General-purpose output UART Transmit Data Out (TXD) PLL Mode select, Bit 1 (sampled during Reset)
51	**P0_2** PLL_FMODE_0 TDO TDO_FLASH	O/PU	General-purpose output PLL Mode select, Bit 0 (sampled during Reset) Microcontroller JTAG Debug interface TDO signal Flash JTAG programming interface TDO signal
52	**P0_1** FMODE_2 RTCK TOEN_FLASH	O/PU	General-purpose output Functional Mode select, Bit 2 (sampled during Reset) Microcontroller JTAG Debug interface RTCK signal Flash JTAG programming interface TOEN signal
53	**P0_0** T3 TRST_FLASH	IO/PU	General-purpose input/output Timer T3 external clock or gated clock input Flash JTAG programming interface TRST signal
54	**P1_7** AdcExtTrig INT4	IO/PU	General-purpose input/output ADC External Trigger input External Interrupt input
55	**VDD33**	Power	+3.3V Supply voltage
56	**VSS33**	Power	Digital Ground

4. Electrical Characteristics

4.1 Absolute Maximum Operating Conditions

These are stress ratings only: functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Stresses beyond those listed under "Absolute Maximum Operating Conditions" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Power supply voltage, VDD33 (max) ---------- 3.6V
Power supply voltage, VDD33 (min) ---------- −0.3V
Input voltage, VI (max) ---------- VDD+0.3V, max. 3.6V
Input voltage, VI (min) ---------- −0.3V
Storage temperature range ---------- −40°C to +125°C

4.2 Recommended Operating Conditions

Rating	Symbol	Minimum	Nominal	Maximum	Unit
Power Supply Voltage	VDD33	3.0	3.3	3.6	V
Power Supply Voltage	VDD18	Connect to chip's 1.8V voltage regulator output VOUT18			V
Total Maximum Supply Current	IDD_{33max}	no load on digital outputs		500	mA DC
Average Power Consumption	IDD_{33avg}	During Reception	75		mA DC
High Level Input Voltage	V_{IH}	2		VDD+0.3 / 3.6	V
Low Level Input Voltage	V_{IL}	0		0.8	V
High Level Output Voltage [1]	V_{OH}	at I_{DOmax}		3.5	V
Low Level Output Voltage [1]	V_{OL}	at I_{DOmax}		0.4	V
Source and Sink Current [2]	I_{DO}	Max. 5 I/Os at same time		8	mA
Internal Operating Frequency	F_{OSC}		46.08		MHz
Crystal Overall Accuracy			120		PPM
Operating Temperature Range	T_0	−40	25	+85	°C

Note: [1] At maximum sink/source current
[2] Digital I/O pins, max. 5 outputs sink/source at the same time

5. Chip Configuration

5.1 Phase Locked Loop (PLL)

The IT700 has an integrated Phase Locked Loop (PLL) circuit that allows operating the device with different input clock frequencies.

The PLL operating mode is determined by sampling pins PLL_FMODE_1 (P0_3) and PLL_FMODE_0 (P0_2) during Reset. Table 3 shows the different PLL configurations and the required crystal input clock frequency for each mode.

Table 3: PLL Mode Selection

PLL_FMODE_1 (P0_3)	PLL_FMODE_0 (P0_2)	PLL state	Crystal Frequency [MHz]	PLL OUT [MHz]
1	1	active	5.12	46.08
0	1	active	15.36	46.08
1	0	active	15.36	46.08
0	0	Power down	46.08	Bypassed

5.2 IT700 Operating Modes

The IT700 chip operating mode is determined by sampling pins FMODE_0 (P2_1), FMODE_1 (P2_2) and FMODE_2 (P0_1) during Reset. Those pins are internally pulled high, which defaults to selecting the Protocol Controller Architecture mode. Do **not** pull these pins low during Reset.

Table 4: IT700 Operating Mode Selection

FMODE_2 (P0_2)	FMODE_1 (P2_2)	FMODE_0 (P2_1)	Mode
1	1	1	Protocol Controller Architecture Mode

6. Host Interface

The IT700 Protocol Controller Architecture version comes with Yitran's Network layer pre-programmed into the integrated 8051 microcontroller's Flash memory. In this mode the device operates as a "closed" PLC modem chip. An external host and application controller is required to implement your application layer functionality. The host controller connects to the IT700 through a UART interface (RXD and TXD pins) with 38400 bps, 8 data bits, odd parity, 1 stop bit an no flow control.

Figure 3 shows the typical schematic connections for the IT700 Protocol Controller Architecture.

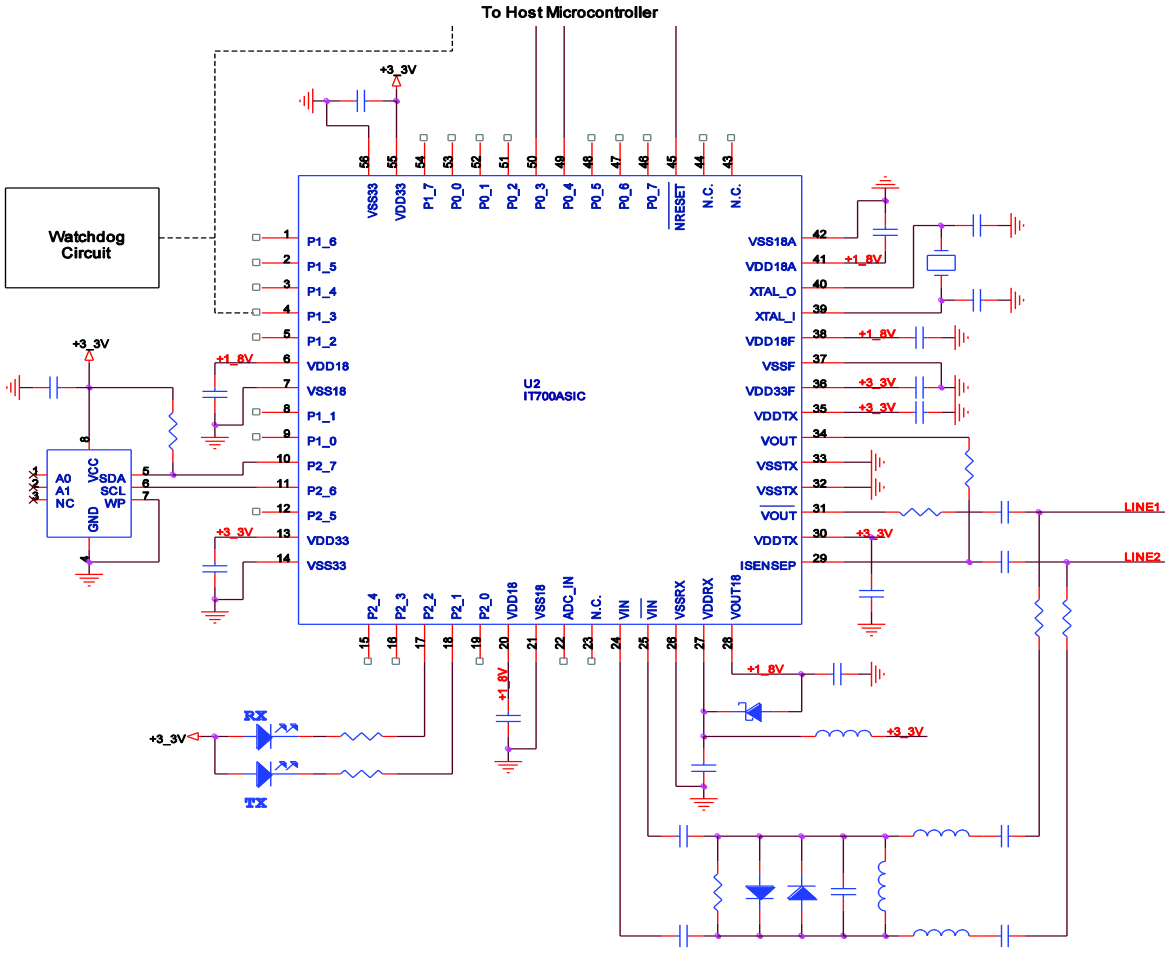

Figure 3: Typical Application Circuit, IT700 Protocol Controller Architecture

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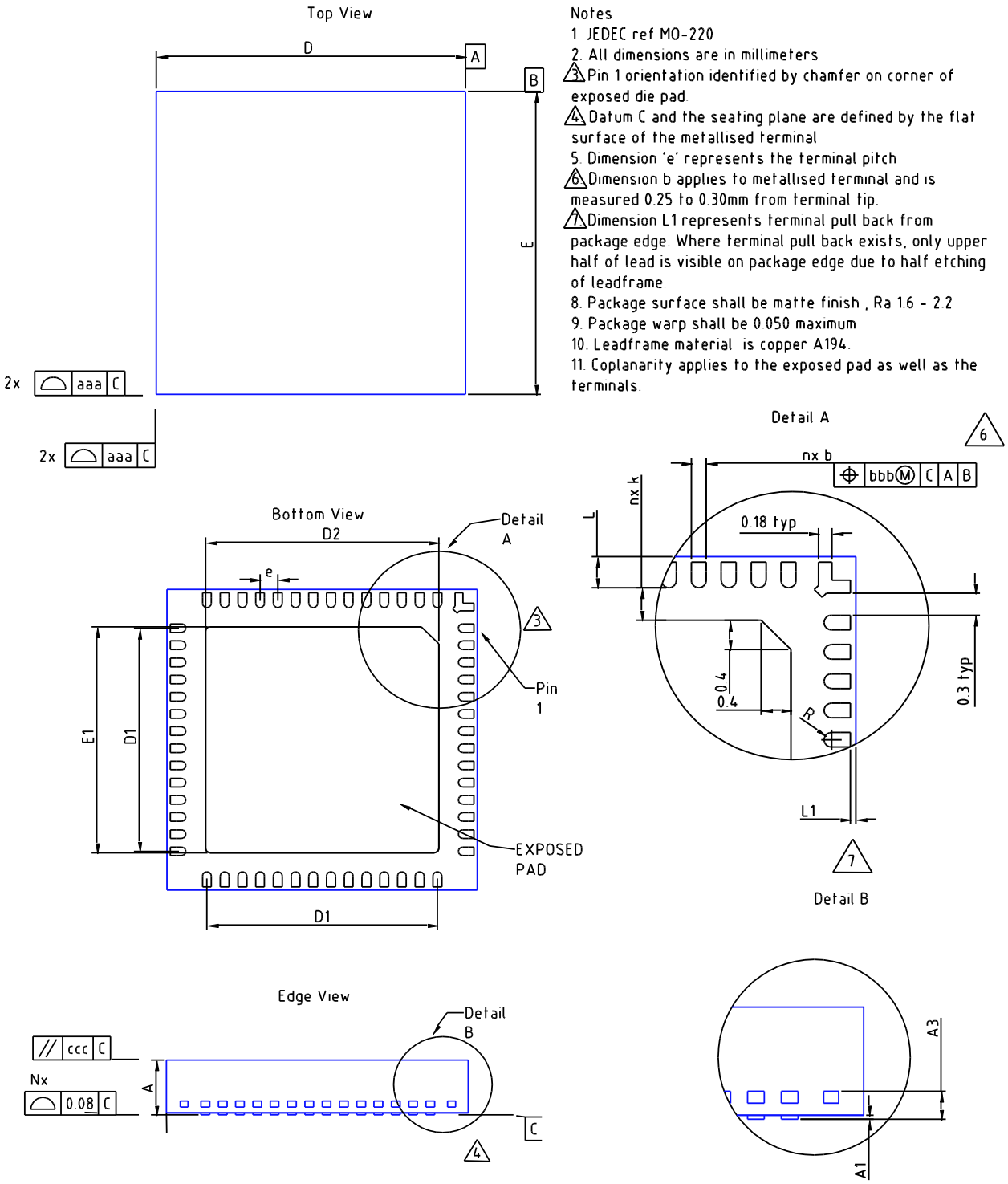
7. Mechanical Dimensions



Notes
1. JEDEC ref MO-220
2. All dimensions are in millimeters
3. Pin 1 orientation identified by chamfer on corner of exposed die pad.
4. Datum C and the seating plane are defined by the flat surface of the metallised terminal
5. Dimension 'e' represents the terminal pitch
6. Dimension b applies to metallised terminal and is measured 0.25 to 0.30mm from terminal tip.
7. Dimension L1 represents terminal pull back from package edge. Where terminal pull back exists, only upper half of lead is visible on package edge due to half etching of leadframe.
8. Package surface shall be matte finish , Ra 1.6 - 2.2
9. Package warp shall be 0.050 maximum
10. Leadframe material is copper A194.
11. Coplanarity applies to the exposed pad as well as the terminals.

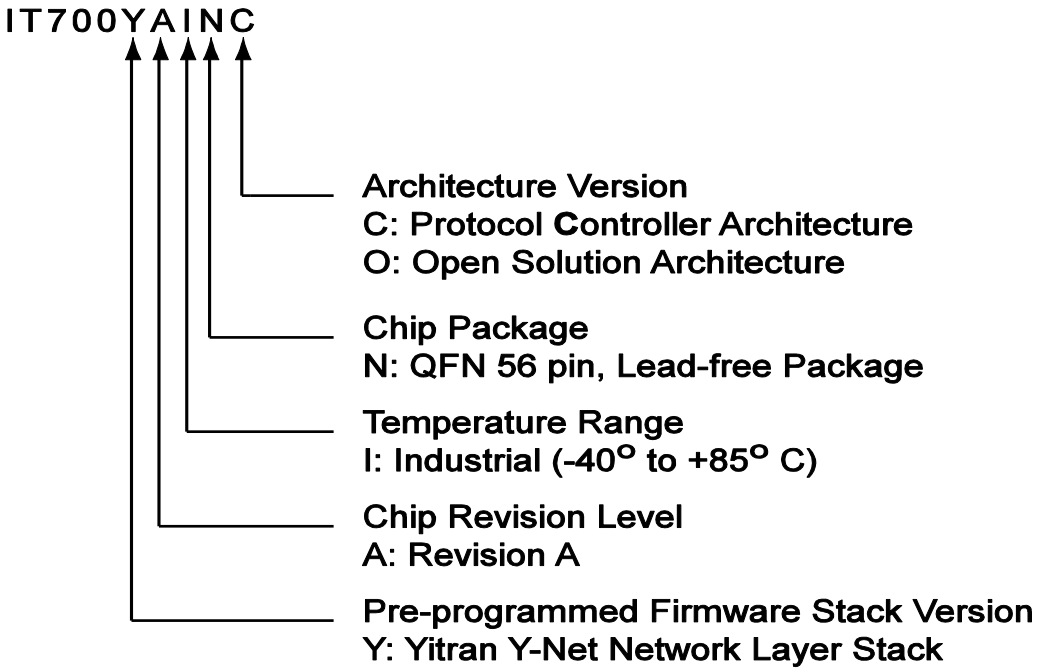
7.1 Package Tolerances

Common Dimensions (mm)			
Symbol	**Min**	**Nom**	**Max**
A	0.85	0.9	1
A1	0	0.02	0.05
A3		.20 ref	
D	6.9	7	7.1
D1		5.2	
D2	5.2	5.3	5.4
E	6.9	7	7.1
E1		5.2	
E2	5.2	5.3	5.4
L	0.3	0.4	0.5
L1			0.1
b	0.15	0.2	0.25
N		56	
e		0.4	
k	0.2		
R	b min/2		
T		0.15	

Tolerances for Form & Position (mm)	
Symbol	**Value**
aaa	0.1
bbb	0.07
ccc	0.1

8. Ordering Information

The IT700 part naming convention for ordering parts is shown below:



Document Control

Rev	Date	Description
1.0		
1.1		
1.2		
1.3	1 March 2009	Operating Conditions section updated IT700 Protocol Controller Architecture figure updated IT700 Pin Description table updated
1.4	September 2014	Document format change
1.5	November 2016	Notice update

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